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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/674,082	09/29/2003	Jayesh R. Bhakta	NETL.001DV2	2166

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EXAMINER	
PHAM, LY D	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 08/18/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/674,082	BHAKTA ET AL.	
	Examiner	Art Unit	
	Ly D Pham	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *120303 & 040104*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Applicant's Pre-Amendment filed January 30, 2004 has been entered. The specification and claims 1 and 6 – 8 have been amended. New claims 10 – 18 have been added.

2. Applicant's Information Disclosure Statements, IDSs, filed December 03, 2003 and April 01, 2004 have been considered by the Examiner.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Perego et al. (US Pat 6,502,161 B1).

Regarding **claims 1 and 10 – 12**, Perego et al. disclose a memory module comprising:

a printed circuit board having a line of bilateral symmetry which bisects the printed circuit board into a first lateral half and a second lateral half of at least one surface of the PCB (figs. 4A, 4B, 4C, and 7, which show the IC chips being arranged bilaterally symmetric with respect to the buffers in the middle);

a plurality of identical ICs mounted in a first row (fig. 7, any bottom row of any memory module) and a second row onto at least one surface of the PCB (fig. 7, any top row of any memory module);

a control logic bus connected to the plurality of identical integrated circuits (col. 1, lines 26 – 34, '... control/address bus, data bus, ...').

As per the claimed feature in which a first addressing register coupled to the ICs of the first lateral half and a second addressing register coupled to the ICs of the second lateral half, in stead of having two separate chips, Perego et al. disclose a buffer for accessing the ICs in a combined fashion, which means a single chip buffering the two rows of ICs. For the identical and practical purpose of addressing the memory chips, semiconductor fabrication for circuit combination is common and well known in the art to optimize space. Therefore, it is considered obvious to one of ordinary skill in the art, at the time the invention was made, to realize the variations of design from the scope disclosed by Perego et al. as exemplified by the claimed features, all of which can be viewed as slight modifications from design preferences.

From another view point, although Perego et al. did not clearly show two separate registers for addressing the ICs of the first and second lateral portions, respectively, it would have been obvious to one having ordinary skill in the art at the time the invention was made to implement the two address registers as claimed as opposed to a single chip address control buffer for addressing subsets of memory modules (col. 1, line 65 – col. 2, line 11) since it has been held that constructing a formerly integral structure in various elements involves only routine skill in the art. *Nerwin v. Erlichman*, 168 USPQ 177, 179.

Regarding **claim 3**, although Perego et al. did not show the PCB having approximate dimensions of 5.25 inches wide by 2.05 inches high, it would have been an obvious matter of design choice to arrive at such dimension approximation as claimed since such a modification would have involved a mere change in the size of a component. A change in size is generally recognized as being within the level of ordinary skill in the art. *In re Rose*, 105 USPQ 237 (CCPA 1955).

5. Claims 2, 4, and 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Perego et al. (US Pat 6,502,161 B1) in view of Li et al. (US Pat 6,705,877 B1).

Regarding **claims 2, 4, and 5**, though Perego et al. did not clearly disclose the memory module further having the features as claimed in claims 2 – 5, however, Li et al. show TSOP memory modules (col. 5, lines 12 – 15) comprising integrated circuits of types 256-Megabit or 512-Megabit SDRAM (col. 6, lines 26 – 36), in which DDR SDRAM type is one option (abstract), to constitute a 1-Gigabyte and 2-Gigabyte capacity memory modules, respectively. Therefore, it is considered obvious to one of ordinary skill in the art, at the time the invention was made to include such feature to the disclosure by Li et al. so that upgrading different memory capacity configuration becomes possible (col. 3, lines 1 – 3).

6. Claims 6 – 9 and 13 – 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Perego et al. (US Pat 6,502,161 B1) in view of Yamasaki et al. (US Pat 6,594,167B1).

Regarding **claims 6 – 9 and 13 – 18**, Although Perego et al. did not clearly teach the feature in which the ICs on the second row are oriented 180 degrees with respect to the first row, the feature is however shown by Yamasaki et al. (fig. 13, chips over the centerline 1 are oriented 180 degrees opposite to chips under the centerline 1). Therefore, it is considered obvious to one of ordinary skill in the art, at the time the invention was made, to include the feature shown by Yamasaki et al. to the invention by Perego et al. so that I/O pins of the chips may be nearest to the center line of the module substrate parallel to a connect pin group, which yields substantial equal interconnection lengths between the respective memory chips (abstract and Summary of the Invention).

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

8. When responding to the office action, Applicant(s) are advised to provide the examiner with the page and line numbers in the application and/or references cited to assist the examiner to locate the appropriate paragraphs.

9. A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) day from the date of this letter. Failure to respond within the period for response will cause the application to become abandoned (see MPEP 710.02(b)).

10. Any inquiry concerning this communication on earlier communications from the examiner should be directed to Ly Pham, whose telephone number is **571-272-1793**. The examiner can normally be reached on Monday – Friday from 8:30am to 5:00pm, alternate Friday off. The examiner's supervisor, David Nelms, can be reached at **571-272-1787**. The fax number for the organization where this application or proceeding is assigned is 703-872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

Ly Pham LP

August 14, 2004

David Nelms
Supervisory Patent Examiner
Technology Center 2800